What is claimed is:

1. A method of designing patterns, comprising:

preparing a mask pattern used in a lithography process for transferring a circuit pattern intersecting with a step pattern on a substrate which has the step pattern designed thereon; and

applying correction patterns to the mask pattern in accordance with correction rules considering a shape of the step pattern, the correction patterns being applied at intersections of edges of the circuit pattern and the step pattern and in the vicinity of the intersections.

2. The method of claim 1, further comprising preparing the correction rules by use of experiments and lithography simulations, in consideration for at least one of the shape of the step pattern and a shape of the circuit pattern.

3. The method of claim 2, wherein the shape of the step pattern includes at least any one of a height of the step pattern, a line width of the step pattern, a two-dimensional shape of the step pattern and a distance between the step pattern and a step pattern adjacent thereto, and the shape of the circuit pattern includes at least any one of a line width of the circuit pattern, a

two-dimensional shape of the circuit pattern and a distance between the circuit pattern and a circuit pattern adjacent thereto.

4. The method of claim 1, wherein the circuit pattern defines impurity implantation regions.

5. A method of designing patterns, comprising:

preparing a mask pattern used in a lithography process for transferring a circuit pattern intersecting with a step pattern on a substrate which has the step pattern designed thereon;

measuring an amount of footing of edges of the circuit pattern, the footing occurring at one of intersections of the edges of the circuit pattern and the step pattern or the intersections and in the vicinity thereof in executing the lithography process by use of the mask pattern;

preparing correction rules considering a shape of the step pattern;

applying correction patterns to the mask pattern in accordance with the correction rules, the correction patterns being applied at the intersections and in the vicinity of the intersections;

executing process simulations by use of the mask pattern to which the correction patterns are applied;

evaluating operation characteristics of circuit devices, which are obtained by the process simulations; and

reviewing the correction rules until desired operation characteristics are obtained and repeatedly executing the application of the correction patterns and the process simulations.

6. The method of claim 5, wherein the process simulations are impurity implantation simulations.

7. A computer program product for designing patterns, comprising:

instructions configured to prepare a mask pattern used in a lithography process for transferring a circuit pattern intersecting with a step pattern on a substrate which has the step pattern designed thereon; and

instructions configured to apply correction patterns to the mask pattern in accordance with correction rules considering a shape of the step pattern, the correction patterns being applied at intersections of edges of the circuit pattern and the step pattern and in the vicinity of the intersections.

8. The computer program product of claim 7, further comprising instructions configured to prepare the

correction rules by use of experiments and lithography simulations, in consideration for at least one of the shape of the step pattern and a shape of the circuit pattern.

9. The computer program product of claim 8, wherein the shape of the step pattern includes at least any one of a height of the step pattern, a line width of the step pattern, a two-dimensional shape of the step pattern and a distance between the step pattern and a step pattern adjacent thereto, and the shape of the circuit pattern includes at least any one of a line width of the circuit pattern, a two-dimensional shape of the circuit pattern and a distance between the circuit pattern and a circuit pattern adjacent thereto.

10. The computer program product of claim 7, wherein the circuit pattern defines impurity implantation regions.

11. A computer program product for designing patterns, comprising:

instructions configured to prepare a mask pattern used in a lithography process for transferring a circuit pattern intersecting with a step pattern on a substrate which has the step pattern designed thereon;

instructions configured to measure an amount of footing of edges of the circuit pattern, the footing occurring at one of intersections of the edges of the circuit pattern and the step pattern or the intersections and in the vicinity thereof in executing the lithography process by use of the mask pattern;

instructions configured to prepare correction rules considering a shape of the step pattern;

instructions configured to apply correction patterns to the mask pattern in accordance with the correction rules, the correction patterns being applied at the intersections and in the vicinity of the intersections;

instructions configured to execute process simulations by use of the mask pattern to which the correction patterns are applied;

instructions configured to evaluate operation characteristics of circuit devices, which are obtained by the process simulations; and

instructions configured to review the correction rules until desired operation characteristics are obtained and repeatedly executing the application of the correction patterns and the process simulations.

12. The computer program product of claim 11, wherein the process simulations are impurity implantation simulations.

13. A method of manufacturing a semiconductor device, comprising:

preparing a mask pattern used in a lithography process for designing a circuit pattern intersecting with a step pattern on a substrate which has the step pattern designed thereon;

applying correction patterns to the mask pattern in accordance with correction rules considering a shape of the step pattern, the correction patterns being applied at intersections of edges of the circuit pattern and the step pattern and in the vicinity of the intersections; and

forming the circuit pattern on the substrate, by use of the mask pattern to which the correction patterns are applied.

14. The method of claim 13, further comprising preparing the correction rules by use of experiments and lithography simulations, in consideration for at least one of the shape of the step pattern and a shape of the circuit pattern.

15. The method of claim 14, wherein the shape of the step pattern includes at least any one of a height of the step pattern, a line width of the step pattern, a two-dimensional shape of the step pattern and a distance

between the step pattern and a step pattern adjacent thereto, and the shape of the circuit pattern includes at least any one of a line width of the circuit pattern, a two-dimensional shape of the circuit pattern and a distance between the circuit pattern and a circuit pattern adjacent thereto.

16. The method of claim 13, wherein the circuit pattern defines impurity implantation regions.

17. A method of manufacturing a semiconductor device, comprising:

preparing a mask pattern used in a lithography process for transferring a circuit pattern intersecting with a step pattern on a substrate which has the step pattern designed thereon;

measuring an amount of footing of edges of the circuit pattern, the footing occurring at one of intersections of the edges of the circuit pattern and the step pattern or the intersections and in the vicinity thereof in executing the lithography process by use of the mask pattern;

preparing correction rules considering a shape of the step pattern;

applying correction patterns to the mask pattern in accordance with the correction rules, the correction

patterns being applied at the intersections and in the vicinity of the intersections;

executing process simulations of the lithography process by use of the mask pattern to which the correction patterns are applied;

evaluating operation characteristics of circuit devices, which are obtained by the process simulations;

reviewing the correction rules until desired operation characteristics are obtained and repeatedly executing the application of the correction patterns and the process simulations; and

forming the circuit pattern on the substrate, by use of the mask pattern to which the correction patterns are applied, after obtaining the desired operation characteristics.

18. The method of claim 17, wherein the process simulations are impurity implantation simulations.